measurement(s) and production of image(s) carried out for this location vector.

Amend claim 4 as follows:

--4. (Amended) A method as claimed in claim 1, wherein the sequence of location vectors is created from a sequence of vectors, known as test vectors, which is previously formed and recorded, and is designed to make it possible to determine the existence only of a defective gate in the defective circuit, by measurement of the value of the electrical consumption current at rest IDDQ of the defective circuit, and each test vector for which the binary signal of at least one input terminal is liable to change its logic state, is broken down into a plurality of location vectors, the logic state of the binary signals of which does not change.

Amend claim 5 as follows:

--5. (Amended) A method as claimed in claim 1, wherein the sequence of location vectors is created such that two consecutive location vectors are distinguished from one another by the value of a single binary signal applied to a single input terminal.

Amend claim 6 as follows:

--6. (Amended) A method as claimed in claim 1, wherein, in order to measure the value of the electrical consumption current at rest IDDQ of the defective circuit, at least one supply terminal of the defective circuit is applied to the input

of an amplifier circuit (23) which is fitted as a current/voltage converter.

Amend claim 9 as follows:

--9. (Amended) A method as claimed in claim 1, wherein it is determined whether the value measured IDDQ(j) is normal or abnormal, by calculating the standardised difference:

$$D=[IDDQ(j)-IDDQ^{0}(j)]/maximum[IDDQ^{0}(j),Imin]$$

in which

IDDQ(j) is the value measured of the electrical consumption current at rest IDDQ, of the defective circuit with the test vector j;

$IDDQ^{0}(j)$ is the value measured of the electrical consumption current at rest IDDQ, of a standard circuit; and

Imin is a minimum current value which is pre-determined in order to eliminate the effects of noise, the value IDDQ(j) being considered to be abnormal if D is greater than a pre-determined threshold value DS.

Amend claim 11 as follows:

--11. (Amended) A method as claimed in claim 1, wherein, after a first comparison has been made, in which at least one defective area of the surface of the chip has been selected, at least one further comparison is made, only from vector images which correspond to the said defective area.

[Amend claim 12 as follows:]

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--12. (Amended) A method as claimed in claim 1, wherein, for an abnormal location vector, a comparison is made of two sets of images of the defective circuit and/or of a standard circuit, at least one of the two sets of images being a set of vector images which is obtained with the said abnormal location vector, such as to select a defective area in which the defective logic gate can be located, and a further comparison is subsequently made only with the sets of vector images which represent the said defective area.

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[Amend claim 13 as follows:]

--13. (Amended) A method as claimed in claim 1, wherein, during a first comparison of the step of location of the fault, the abnormal vector image used for the image is at least one vector image of a set of vector images, obtained with the first abnormal location vector appearing first in the sequence of location vectors.

[Amend claim 14 as follows:]

--14. (Amended) A method as claimed in claim 13, wherein the electrical functionality of the defective circuit is tested, and, if the defective circuit is found to be non-functional as far as one output terminal at least is concerned, as the reference image, use is made of a vector image, known as the fault reference image (71), obtained with the defective circuit for a location vector, known as the normal location vector, for which

the value measured of the consumption current at rest IDDQ of the defective circuit, is normal.

Amend claim 15 as follows:

--15. (Amended) A method as claimed in claim 14, wherein the fault reference image (71) used is a vector image which is obtained with the defective circuit, in the same sequence of location vectors, with a location vector which precedes the abnormal location vector.

Amend claim 16 as follows:

--16. (Amended) A method as claimed in claim 15, wherein, for a comparison, the abnormal vector image used is a vector image, known as the fault abnormal vector image (70), of the defective circuit, and, in order to compare the fault abnormal vector image (70) and the fault reference image (71), an image is formed, known as the simple fault input image (72, 72'), representing the equipotential lines of the defective circuit which have the same form and the same location, and states of potential which differ between the fault abnormal vector image (70) and the fault reference image (71), such as to be representative of the equipotential input line of the defective logic gate.

Amend claim 18 as follows:

--18. (Amended) A method as claimed in claim 14, wherein, during the step of location of the defective gate, at least one comparison is made between two images of a standard circuit formed from an abnormal vector image, known as the

standard abnormal vector image (76), obtained by applying an abnormal location vector to this standard circuit, and from a reference image, known as the standard reference image (77), obtained by applying a normal location vector to the standard circuit.

Amend claim 21 as follows:

--21. (Amended) A method as claimed in claim 16, wherein, during a further comparison, an image is formed, known as the output image (80), representing the equipotential lines which appear on a simple fault input image (72, 72') or on an intersection fault input image (75), or on a simple standard input/output image (78, 78'), or on an intersection standard input/output image (79); with the exclusion of the equipotential lines which are common amongst these images, this output image (80) representing the equipotential output line of the defective logic gate, and its propagation in the defective circuit.

Amend claim 23 as follows:

--23. (Amended) A method as claimed in claim 1, wherein the electrical functionality of the defective circuit is tested, and, if the defective circuit is found to be functional for all the output terminals, a comparison is made between at least one first abnormal vector image (81) obtained with a first abnormal location vector, and at least one second abnormal vector image (82) obtained with the same circuit, and with a second abnormal location vector which is distinct from the first abnormal

location vector, the first and second abnormal location vectors belonging to the same sequence of location vectors.

Amend claim 26 as follows:

--26. (Amended) A method as claimed in claim 25, wherein, in a further comparison, an image is formed, known as the output image (86), which represents the equipotential lines common to the fault output image (83) and to the intermediate output image (85), the said output image (86) representing the equipotential output line of the defective logic gate.

Amend claim 27 as follows:

--27. (Amended) A method as claimed in claim 1, wherein the test images are produced by electronic scanning microscopy with contrast of potential, by detection of the secondary electrons.

Amend claim 28 as follows:

--28. (Amended) A method as claimed in claim 1, wherein the vector images are recorded in monochrome pixelised form, and each comparison is made between images in pixelised form, numerically, pixel by pixel.

Amend claim 30 as follows:

--30. (Amended) A method as claimed in claim 28, wherein, in order to form an image representing the equipotential lines which have the same form and the same location, and states of potential which differ between two initial images, a difference

in the two initial images is produced pixel by pixel, according to the formula:

$$PC=(PA-PB)/2+INT(E/2)$$

in which PA is the value of the contrast level of the pixel of the first input image; PB is the value of the contrast level of the pixel of the second input image; E is the maximum value of the contrast level of the images; PC is the value of the contrast level of the pixel of the image formed; and INT is the whole part function.

Amend claim 32 as follows:

--32. (Amended) A method as claimed in claim 28, wherein, in order to form an image which represents the equipotential lines of one or the other of two initial images, with the exclusion of the equipotential lines which are common to these two initial images, there are carried out:

- a thresholding step, which adapts to three contrast levels, i.e. white, black and grey; and
- pixel by pixel, an extended exclusive OR comparison, XOR+, during which the following contrast levels are allocated to each pixel of the image to be formed:

. grey, if the two pixels of the initial images have the same contrast value on completion of the adaptive thresholding;